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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/549,850	09/23/2005	Arnaud Dahamel	034512-001	7093

21839 7590 06/18/2009

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EXAMINER	
SQUIRES, BRETT S	

ART UNIT	PAPER NUMBER
2431	

NOTIFICATION DATE	DELIVERY MODE
06/18/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ADIPFDD@bipc.com

Office Action Summary	Application No.	Applicant(s)	
	10/549,850	DAHAMEL ET AL.	
	Examiner	Art Unit	
	BRETT SQUIRES	2431	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 March 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in France on March 24, 2003. It is noted, however, that applicant has not filed a certified copy of the FR 03/03522 application as required by 35 U.S.C. 119(b). The applicant has instead submitted a certified copy of foreign application FR 02/02848 filed in France on March 6, 2002 and titled "Shelter for Fruit Trees Comprising Abutted Greenhouse Units Rigidified with Rigging and Equipped with Means for Tensioned Unfolding or Foldable Roofs." The foreign application FR 02/02848 filed March 6, 2002 does not support the applicant's claim for foreign priority.

Claim Objections

2. Claim 16 is objected to because of the following informalities: claim 16 recites "said length greater," on page 3 line 20, "the standard length," on page 3 line 20, and "said length," on page 3 line 22. It is unclear which length is being referred to by the claim language "said length." Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 12-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Ma et al. (US 6,996,725).

Regarding Claim 15:

Ma discloses an integrated circuit (“Microcontroller" See fig. 2A ref. no. 100) having a microprocessor ("CPU” See fig. 2A ref. no. 235), a set of peripheral devices connected to the microprocessor (“Data Encryptor," "Program Decryptor," "Instruction Cache," and "Boot ROM" See fig. 4 ref. nos. 230, 400, and 420) by a bus (“Internal data bus” See fig. 4 ref. no. 240D and fig. 6 ref. no. 210) having a data length equal to the standard length of data processed by the microprocessor (“Internal data bus 240D is 8-bits wide" See col. 6 lines 47-48 and “The CPU processes one byte instructions.” See col. 2 lines 6-34), a security module connected to the bus for encrypting and decrypting data (“Decryptor” See fig. 2A ref. no. 220, col. 3 lines 36-39, col. 5 lines 46-67 and col. 6 lines12-24), a communication interface for accessing devices external to the integrated circuit (“I/O Buffer” See figs 2A and 4 ref. no. 215), the communication interface being connected to the security module by a dedicated link that is distinct from the bus ("The connection between the Decryptor and the I/O Buffer." See figure 2A), such that data exchanged between the microprocessor and the communication interface is encrypted and decrypted by the security module (“The microcontroller 100 is able to transfer (e.g., encrypted) information over the bus 210 from the external memory 205 into the I/O buffer 215, where the encrypted information is held until it is forwarded to the decryptor 220.” See col. 4 lines 27-30), a cache memory (“Decrypted Buffer” See figs. 2b ref. no. 225 and fig. 4 ref. no. 400DB) that stores data to be provided to the security module for

encryption and transfer to an external device via the communication interface ("It should also be understood that the decryptor 400D may also optionally include encrypting functions," See col. 10 lines 2-9), and a cache memory controller ("Memory Controller" See fig. 4 ref. no. 405) that writes data to the cache memory in units each having a length greater than the standard data length of the data processed by the microprocessor for encryption by the security module ("After a reset, the memory controller may begin fetching program code from the external memory. Eight consecutive external addresses are generated by the address generator 415 (illustrated in fig. 4) to fetch eight bytes of code to the encrypted buffer 400EB." See col. 9 lines 62-67 and col. 10 lines 1-4).

Regarding Claim 12:

Ma discloses during the deciphering of the data by the security module, the cache memory breaks the deciphered data available at the output of the security module which has a length greater than the standard data length into standard-length data ("The CPU may wait until the decrypted instructions are stored in the cache and then the cache transmits a one byte instruction to the CPU upon request by the CPU." See col. 2 lines 6-34 and col. 5 lines 20-23 and "The decrypted buffer 225 may also be couple to CPU/instruction decoder 235 (e.g. via the internal bus 240, another bus (not illustrated), etc.) to enable cache bypassing. See col. 4 lines 23-26).

Regarding Claim 13:

Ma discloses decryptor uses a secret key algorithm which processes data having a length of at least 64-bits and wherein the standard length of the data processed by the

microprocessor is less than 64-bits ("The CPU processes one byte instructions." See col. 2 lines 6-34 and "The microcontroller may be designed to decrypt a 64-bit block in five machine cycles for single DES operations." See col. 6 lines 25-34).

Regarding Claim 14:

Ma discloses a block encryption scheme using the AES algorithm (See col. 3 lines 20-25).

Regarding Claim 16:

Ma discloses the security module decrypts data received from an external device via the communication interface in units that are equal to the length greater than the standard length ("Program decryption, on the other hand, may be effectuated on blocks of 64 bits through program decryptor 400." See col. 6 lines 25-34), and provides the decrypted data to the cache memory controller for writing to the cache in units of the length ("The 64-bit block of encrypted code is then decrypted with the decryptor 400D, with the results being placed in the decrypted buffer 400DB." See col. 10 lines 1-9).

Response to Arguments

5. Applicant's arguments filed March 2, 2009 have been fully considered but they are not persuasive.

In response to applicants' argument that data to be encrypted and transferred to an external device, such as memory, is written into a cache memory in units having a length greater than the standard length of data processed by the microprocessor, the examiner respectfully points out that the decrypted buffer has the same structure as the

claimed cache memory in that the decrypted buffer stores 64-bit blocks of decrypted instructions for the CPU (See col. 10 lines 2-4) and can be coupled to the CPU (See col. 4 lines 23-26). Accordingly, the naming convention cache memory does not distinguish the claimed memory element from the decrypted buffer disclosed by Ma.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRETT SQUIRES whose telephone number is (571) 272-8021. The examiner can normally be reached on 9:30am - 6:00pm Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Korzuch can be reached on (571) 272-7589. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/BS/

/William R. Korzuch/
Supervisory Patent Examiner, Art Unit 2431